concurrently with this amendment. In view of the claims as amended and the following remarks, it is submitted that the application is now in the condition for allowance.

Canceled claims 56,57,58,60,67,68,69 and 71 were rejected under 35 U.S.C. § 112, second paragraph because of the word "same." That objection cannot be made against the new claims.

Canceled claims 52-58, 62, 65-69 and 73 were rejected unde4 35 U.S.C. §102(b) as being anticipated by Pruniaux et al. (3,823,352). That rejection does not apply to the new claims.

Pruniaux's patent shows a mesa device. The claims as amended do not read on a mesa device. The reference fails to show or suggest forming well and source regions in the first surface, forming a drain layer in the substrate, and forming gate regions between the source regions and the drain layer. The amendment is supported in the specification and the drawings by the wells 56, 76, the sources 22, 57, 77 and the gates 54, 55 and 74, 75.

The new claims call for a plurality of sources connected together and a plurality of gates connected together. That defines the cellular structure of the IGBT or MOSFET. In contrast, Pruniaux shows a conventional transistor with one source and one gate. Pruniaux fails to show a process for having multiple sources and multiple gates connected together.

The new claims call for a pattern of recesses in the second surface of the substrate. Pruniaux does not show a pattern of recesses in the second surface.

Claims 86 and 97 are further distinguished from Pruniaux by the recitation of a lower limit of "not less than about 0.4 percent." Prunaiux fails to show or suggest that limit. Claims 88, 89, 99 and 100 are distinguished from Prunaiux because it fails to show or suggest an array of recesses, in particular a grid array of recesses. The drain contact/heat sink 16 is a single contact. It is not an array. Prunaiux fails to show more than one drain contact/heat sink under its device.

The new claims are not anticipated by Okabe, et al. (U. S. Patent No. 5,663,096).

Okabe has no recesses and thus fails to show the claimed recesses in the second surface of the substrate. Because Okabe has no recesses, it likewise fails to show resistivity lowering bodies in recesses.

The last office action equated the the rough surface 22 of Okabe to the recesses of the claims. Applicant submits that the surface 22 is simply that, a rough surface and it does not include recesses as set forth in the claims.

The drawings in Okabe show a rough surface to indicate that the lower surface of the wafer is rough after it has been thinned by an abrasive removal process. Okabe teaches the use of a grindstone 18 as shown in Fig. 3 for removing material from the back surface. Okabe nowhere uses the term "recess" in his disclosure.

Applicant submits that the Examiner, as one skilled in the art, will recognize the difference between recesses that are intentionally formed in a surface and a randomly roughened surface that results from an abrasive operation.

The new claims contain limitations that cannot be equated to a rough surface. Okabe fails to show or suggest "a pattern of recesses extending from the second surface of the substrate into interior portions of the semiconductor substrate." Okabe also fails to show "recesses located at chosen positions." Okabe is silent about the shape of damaged areas of its rough surface and does not provide for the "chosen shapes and chosen depths in the substrate" of the claimed recesses. In summary, the pattern of defined, structured, and placed recesses is not shown or suggested by Okabe.

Because Okabe does not form recesses, it is not available as a reference against the remaining dependent claims 77-93 and 95-104. More specifically, Okabe fails to show or suggest "sawing or etching a recess into the surface of the substrate" or "laser etching to form cylindrical recesses" or a "repeated pattern", in particular a "trapezoidal pattern"or "a grid of intersecting trenches."

Claims 94-104 are also distinguished from Okabe on grounds that Okabe does not show resistivity lowering bodies extending from the second surface of the substrate. As pointed out above, there are no recesses in Okabe and thus, the ohmic electrode 26 is necessarily formed only on the surface 22.

Okabe fails to show the subject matter of claims claims 85 and 96. Okabe is silent about platinum or silver. Likewise, the only mention of gold in Okabe is for the outermost or top layer on the back substrate. That top layer is not a resistive body and certainly is not below the surface of the substrate.

Okabe does not show the invention of claims 86 and 97. For the same reasons

given above, Okabe does not show or suggest resistivity-lowering bodies. Instead, the Okabe structure would likely generate a graph similar to the diamond graph shown in Figs. 7-14.

Okabe does not show the invention of claims 88-90 and 99-101. The rotational lapping operation performed Okabe does not generate a grid pattern. A grid by definition includes parallel lines. Okabe fails to show or suggest any grid pattern of parallel lines. Indeed, the Examiner, as one skilled in the art, knows that a rotating abrasive grinding tool applied to a surface does not produce trenches or grids. The abraded area has a patina of scratches, but has no pattern. In this regard, Applicant points out that Okabe never identifies any trenches or grid, per se, in its text. Instead, reference number 22 is directed to an abraded surface.

Claims 92, 93, 103 and 104 are not shown or suggested by a combination of Pruniaux and Okabe who mentions using its process to form an IGBT. As explained above, Pruniaux fails to show or suggest the cellular devices formed by the process. Hence, even if an IGBT were formed with the Pruinaux process, that process would not follow the claimed steps that require multiple sources and multiple gates.

The claims as amended distinguish themselves from the applied art of record. As such, the invention is patentable and a notice of allowance is requested.

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